RK3566_L(VCCIO5 Domain)

U6L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	VOP_BT1120_D0 / SPI1_CS0_M1			/ SDMMC2_D0_M1 /	GPIO3_A1_d	1U5
	VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1 /	GPIO3_A2_d	AR10
	VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1 /	GPIO3_A3_d	AP10
	VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1 /	GPIO3_A4_d	AR9
	VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1 /	GPIO3_A5_d	AP9
	VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1 /	GPIO3_A6_d	1U4
	VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1 /	GPIO3_A7_d	1V3
	VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1 /	GPIO3_B0_d	AR7
PWM8_M0 /	VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/	GPIO3_B1_d	AP7
PWM9_M0 /	VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/	GPIO3_B2_d	AR6
	VOP_BT1120_D9 / I2C5_SCL_M0	/ GMAC1_RXDV_CRS_M0		/ PDM_SDI0_M2 /	GPIO3_B3_d	AP6
	VOP_BT1120_D10 / I2C5_SDA_M0	/ GMAC1_RXER_M0		/ PDM_SDI1_M2 /	GPIO3_B4_d	1U3
PWM10_M0 /	VOP_BT1120_D11 / I2C3_SCL_M1	/ GMAC1_TXD0_M0		/	GPIO3_B5_d	1T4
PWM11_IR_M0 /	VOP_BT1120_D12 / I2C3_SDA_M1	/ GMAC1_TXD1_M0		/	GPIO3_B6_d	1V2
PWM12_M0		/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2 /	GPIO3_B7_d	AP5
PWM13_M0		/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2 /	GPIO3_C0_d	AR4
	VOP_BT1120_D13 / SPI1_MOSI_M1		/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2 /	GPIO3_C1_d	AP4
	VOP_BT1120_D14 / SPI1_MISO_M1		/ UART5_TX_M1	/ I2S1_SDO3_M2 /	GPIO3_C2_d	AP3
	VOP_BT1120_D15 / SPI1_CLK_M1		/ UART5_RX_M1	/ I2S1_SCLK_RX_M2 /	GPIO3_C3_d	AR2
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2 /	GPIO3_C4_d	1P3
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2 /	GPIO3_C5_d	1P4
					VCCIO5_1	1N5
					VCCIO5_2	1N6

RK3566

BGA565_15R50x14R40x0R90

Note:

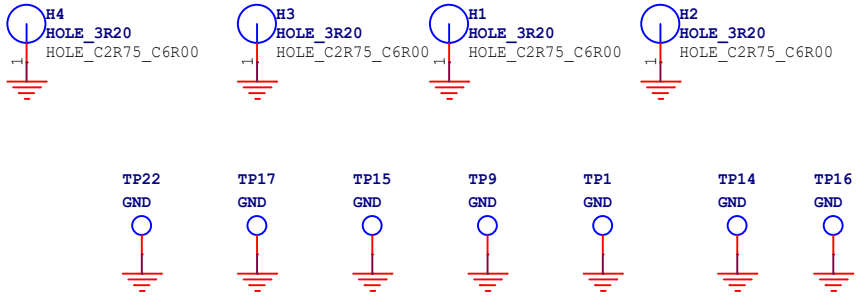
If VCCIO5 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO5 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO5 will be abnormal.

The VCCIO5 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, otherwise the IO of VCCIO5 will be damaged!

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package



TOP Mark

BOTTOM Mark

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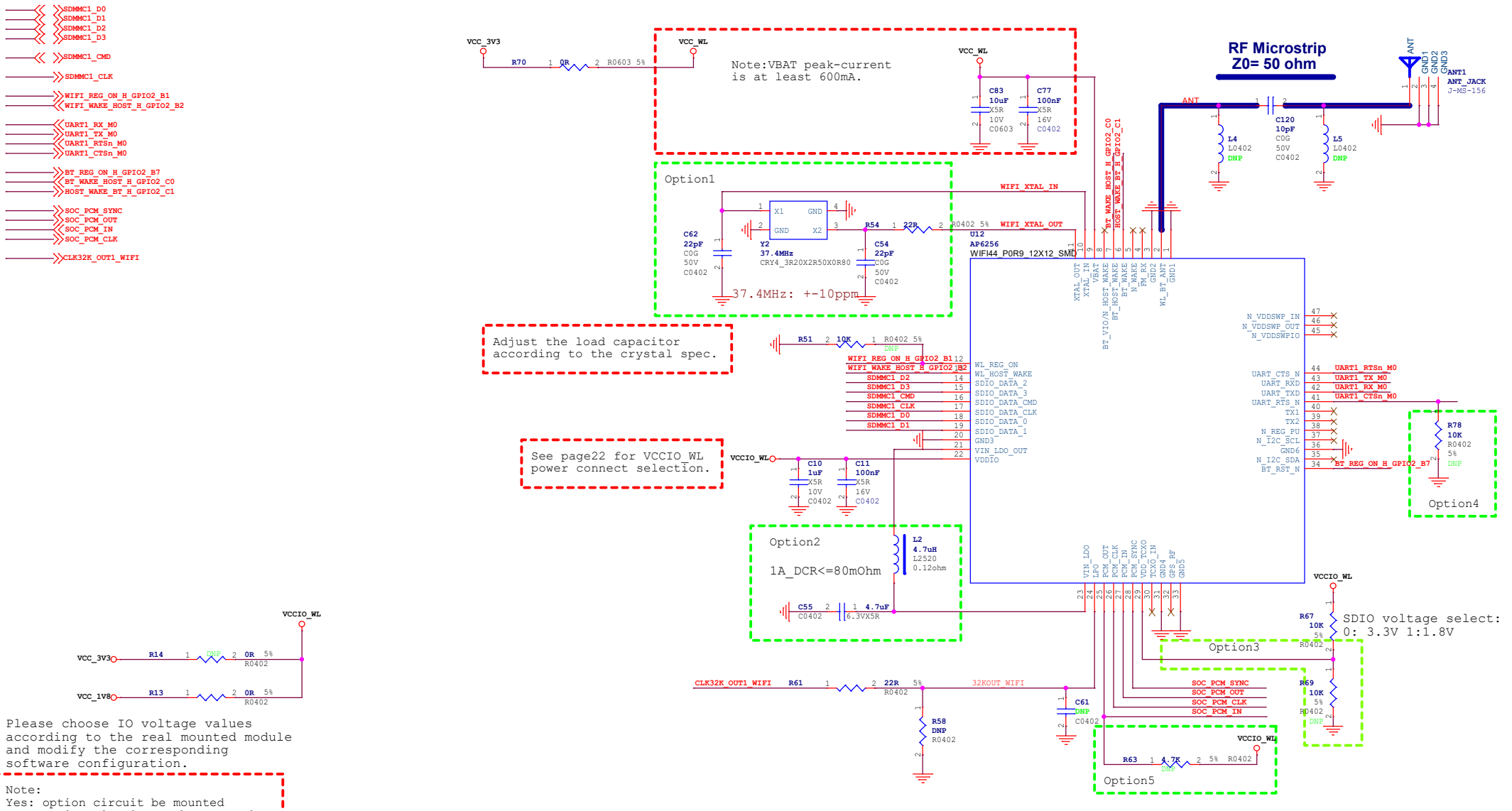
Geniatech Electronics Co., Ltd					
Project:	**RK3566_BOX_Demo1_DDR4P408DD4**				
File:	**29.Mark/Hole/Heatsink**				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	30 of 30



OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3	OPTION4	OPTION5
	a	b/g/n	ac	5GHz								
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	No	No
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	No	No
AP6256/AP6255 Default	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	No	No
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	Yes	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No	No

Geniatech	Geniatech Electronics Co., Ltd			
Project:	RK3566_BOX_Demo1_DDR4P408DD4			
File:	26.WIFI/BT-SDIO1_1T1R + UART			
Date:	Sunday, February 12, 2023		Rev:	<Revision>
Designed by:	<designer>	Reviewed by: <Checker>	Sheet:	27 of 30

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMITX_SCL
HDMITX_SDA
HDMITX_CEC_M0
HDMI_TX_HPDIN

Cj<=0.4pF

U8
STMEF214P101MFR
SON10_2R50X1R00X0R50

U7
STMEF214P101MFR
SON10_2R50X1R00X0R50

HDMI_TX_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TXDDC_SDA_PORT
HDMI_TX_HPD_PORT
VCC5V_HDMI_TX

ED3 ESD5341N ESD0402
ED6 ESD5341N ESD0402
ED5 ESD5341N ESD0402
ED4 ESD5341N ESD0402

C166 1uF X5R 10V C0402

J2
HDMI_TYPE_A
MINI_HDMI_19P_SMT_4DIP
GND D2P D2N GND D1P D1N GND D0P D0N GND CLKP CLKN GND CEC SCL SDA NC +5V HPD
Type C

HDMI TX DDC

VCC5V0_SYS
D9 B5819WS SOD_323
VCC_3V3
R106 10K 5% R0402
Q4 2SK3018 SOT_523
R92 1.8K 5% R0402
HDMITX_SCL
HDMI_TXDDC_SCL_PORT
R107 10K 5% R0402
Q5 2SK3018 SOT_523
R93 1.8K 5% R0402
HDMITX_SDA
HDMI_TXDDC_SDA_PORT

HDMI TX CEC

VCC_3V3 VCC5V0_SYS
R104 27K 5% R0402
Q3 2SK3018 SOT_523
HDMITX_CEC_M0
HDMI_TX_CEC_PORT

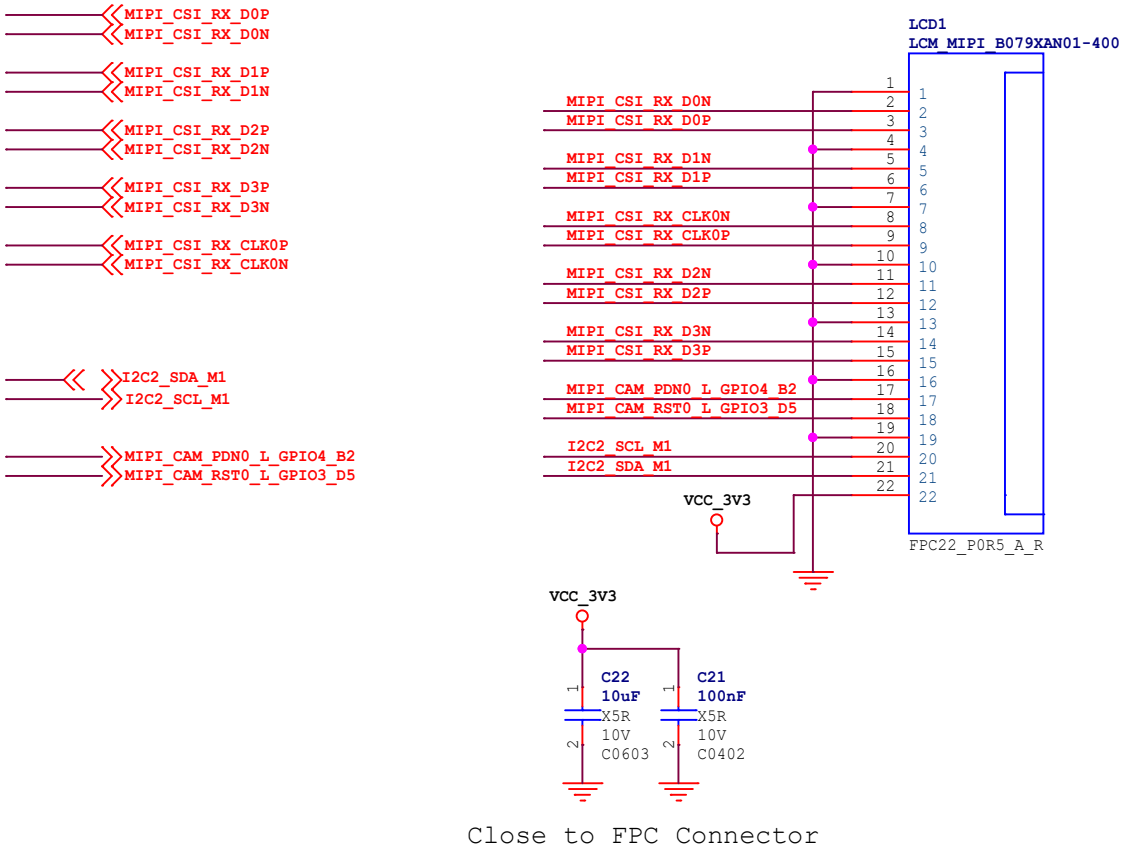
HDMI TX HPD

HDMI_TX_HPDIN R84 1K 5% R0402 HDMI_TX_HPD_PORT
R85 100K 5% R0402

VCC5V0_SYS D10 B5819W SOD_323 VCC5V_HDMI_TX

Geniatech Geniatech Electronics Co., Ltd					
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	25.VO-HDMI2.0 TX				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	26 of 30

MIPI_CSI_RX 4Lanes Interface



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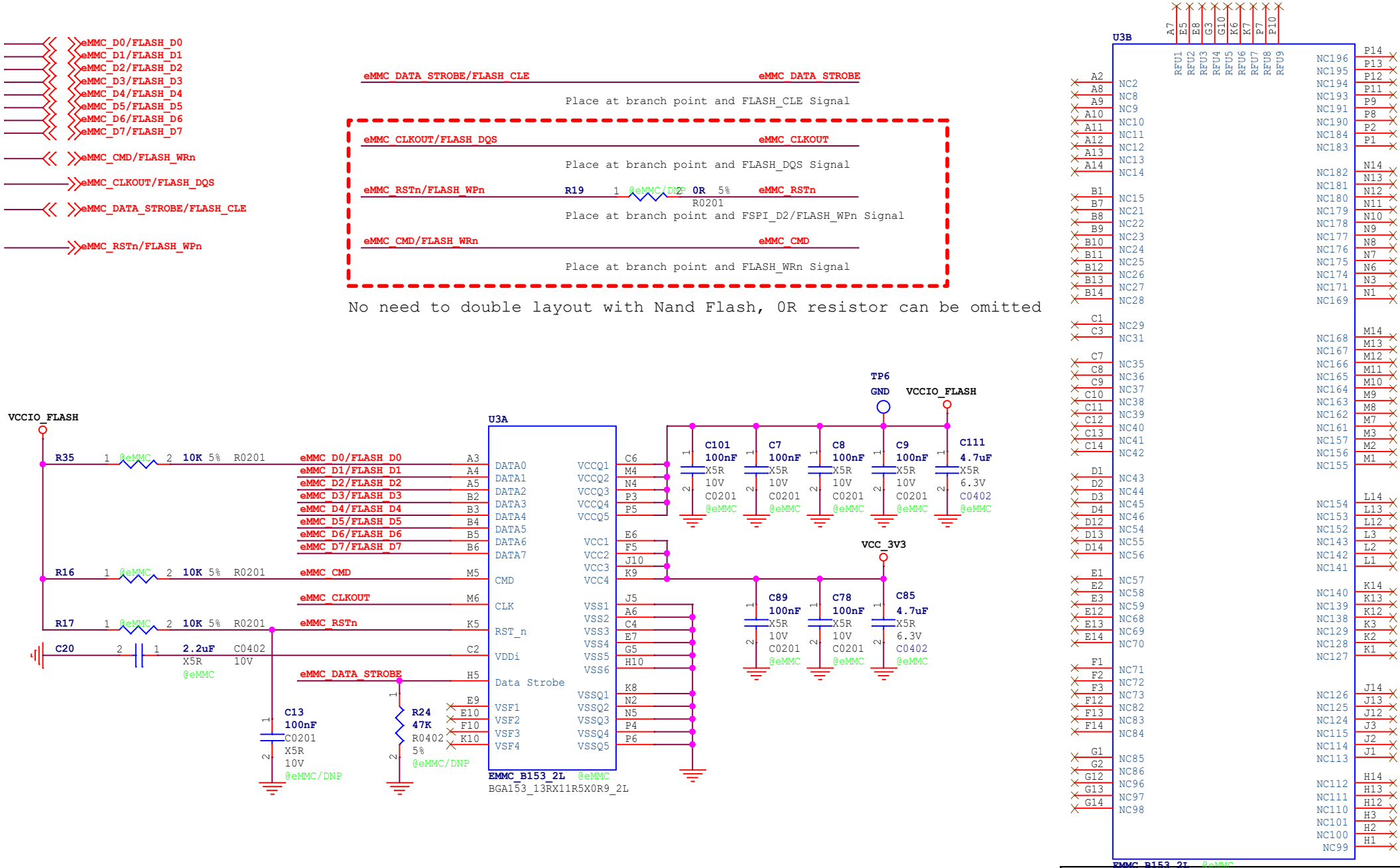
Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	24.VI-Camera_MIPI_CSI_1x 4Lanes				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	25 of 30



If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

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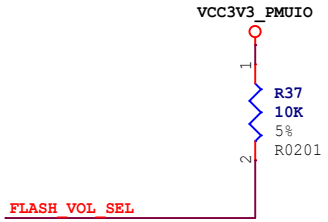
Geniatech Geniatech Electronics Co., Ltd

Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	23.Flash-eMMC Flash				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	24 of 30

FLASH_VOL_SEL

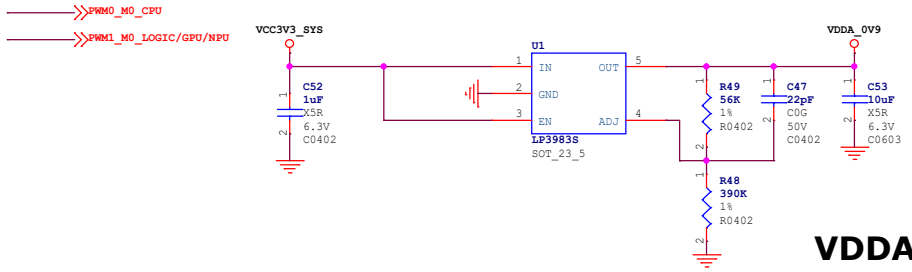
Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)

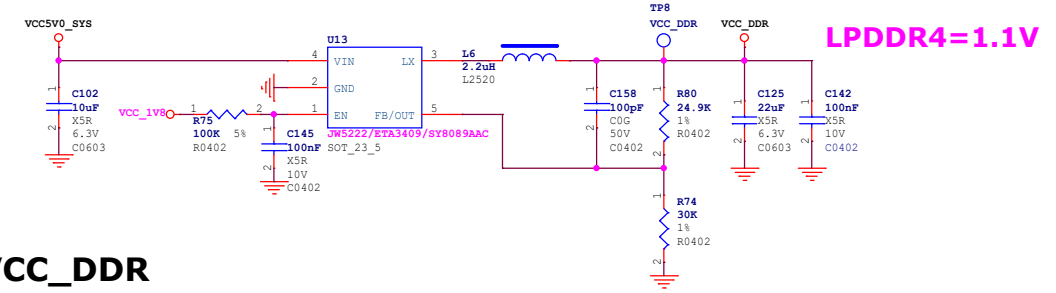


Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

Geniatech Geniatech Electronics Co., Ltd					
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	20.Power_Flash Power Manage				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	21 of 30

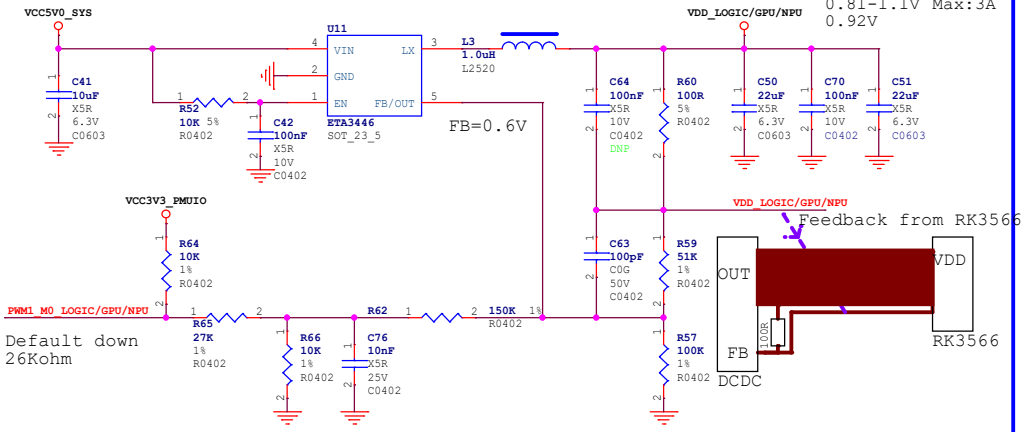


VDDA_0V9

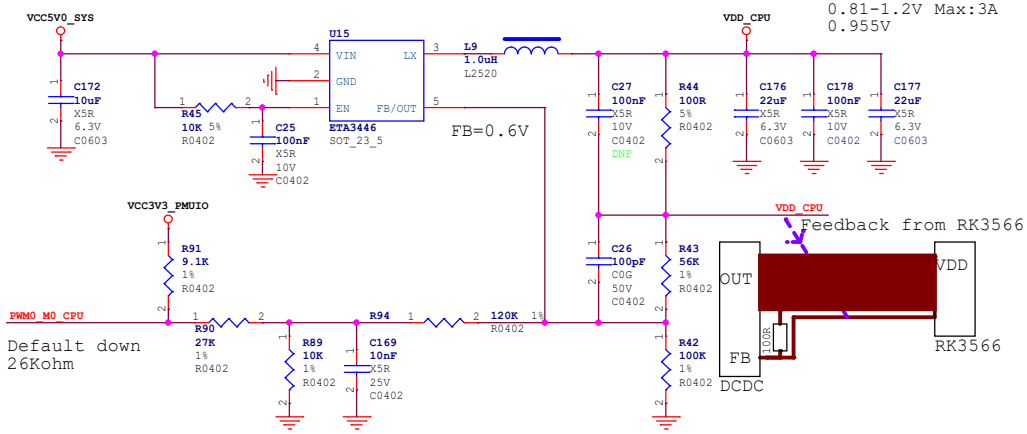


VCC_DDR

VDD_LOGIC/GPU/NPU

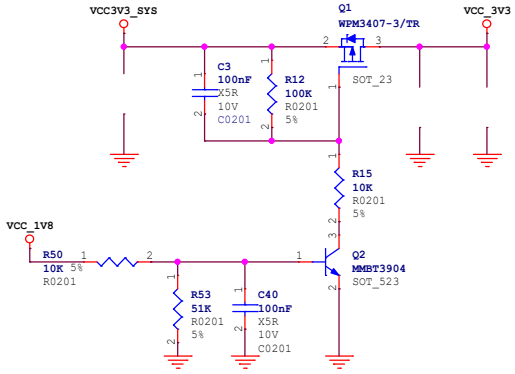


VDD_CPU

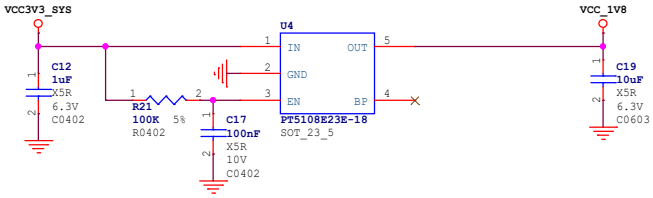


VCC_3V3

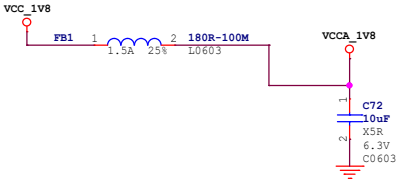
VCC_3V3 power supply has power on timing requirements, can not be deleted!



VCC_1V8



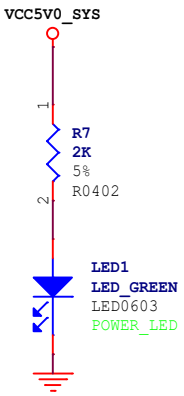
VCCA_1V8



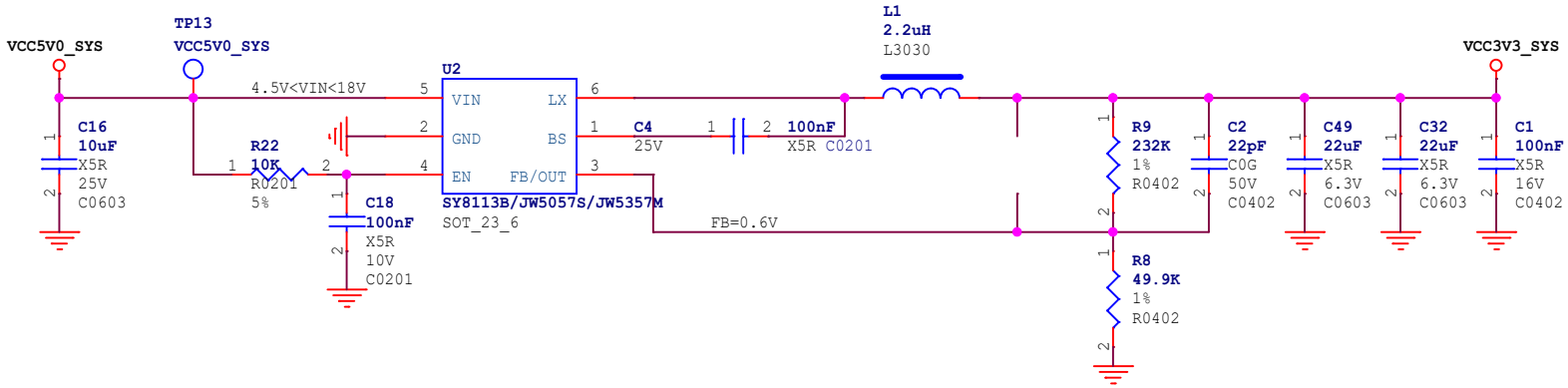
Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	19.Power_DiscretePower				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	20 of 30

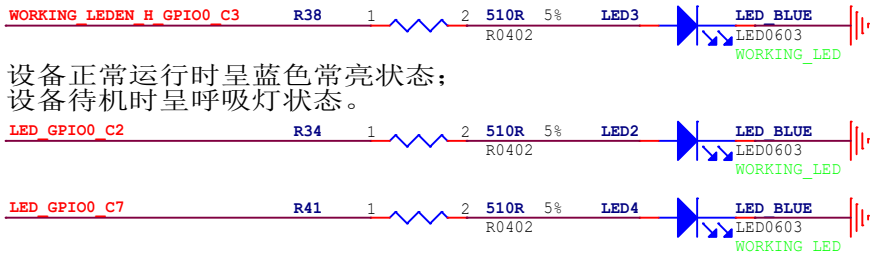
12V/3A DCIN

VCC5V0_SYS

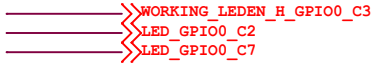


VCC3V3_SYS



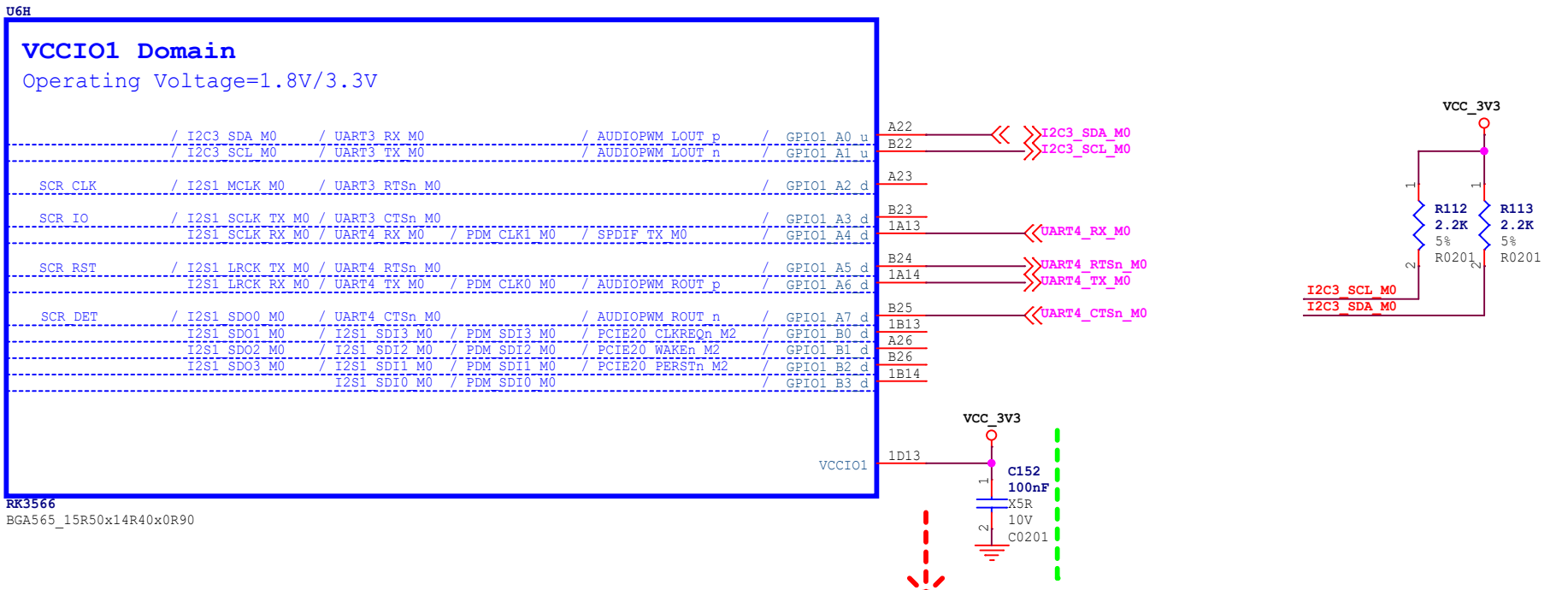


设备正常运行时呈蓝色常亮状态；
设备待机时呈呼吸灯状态。



Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	18.Power_DC IN 12V				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	19 of 30

RK3566_H(VCCIO1 Domain)



Note:

If VCCIO1 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO1 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO1 will be abnormal.

The VCCIO1 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, otherwise the IO of VCCIO1 will be damaged!

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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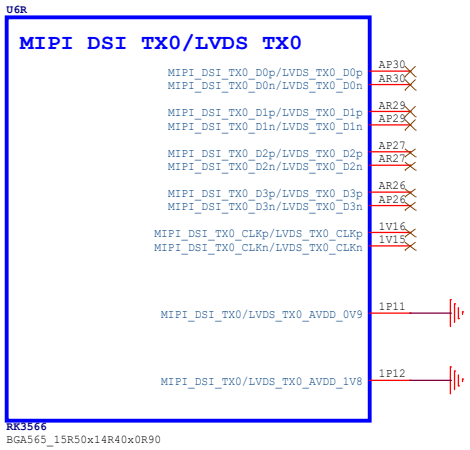
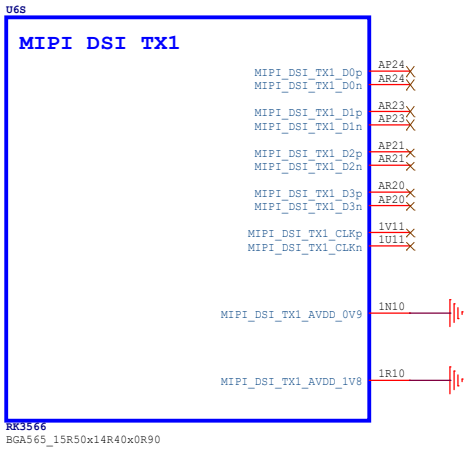
Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	17.RK3566_Audio Interface				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	18 of 30

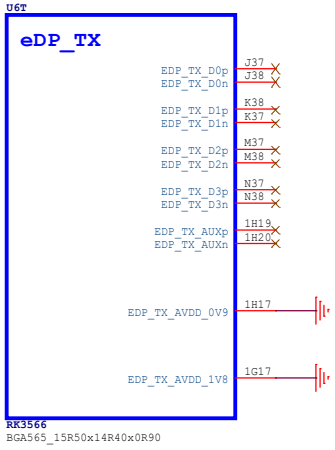
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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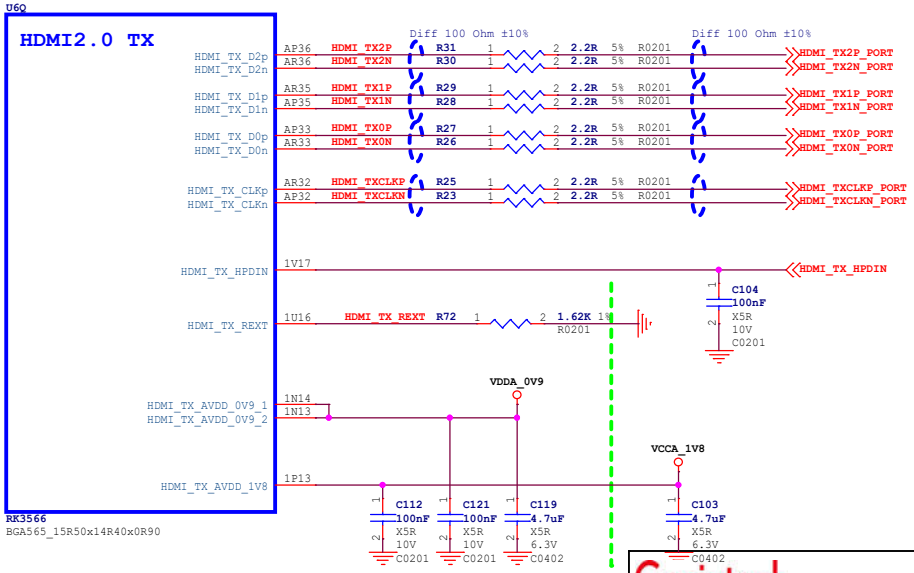
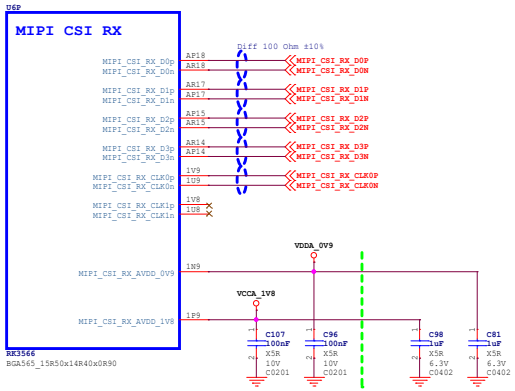
RK3566_Q(HDMI2.0 TX)



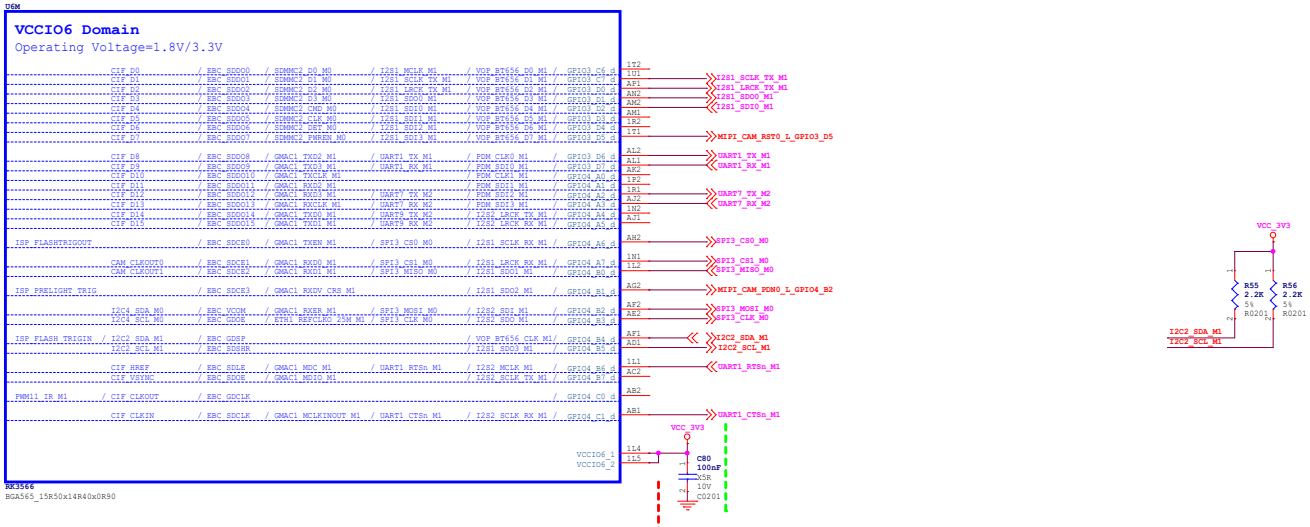
Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	15.RK3566_VO Interface_1				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	16 of 30

RK3566_P(MIPI_CSI_RX)



Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

RK3566_M(VCCIO6 Domain)



Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

Note:
If VCCIO6 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

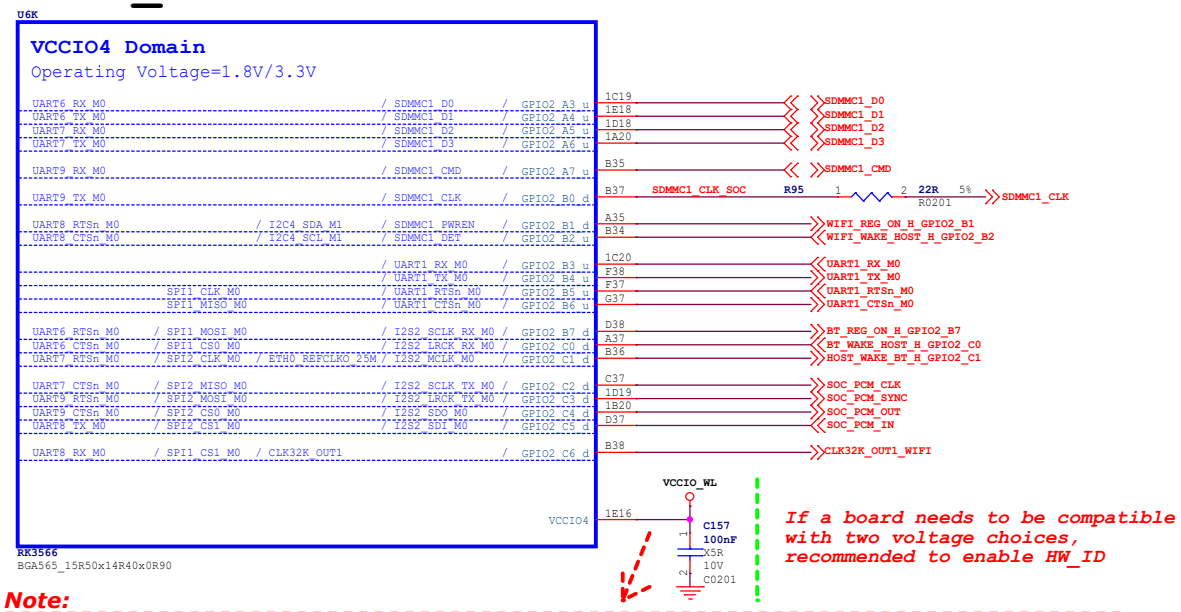
If the VCCIO6 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO6 will be abnormal.

The VCCIO6 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, otherwise the IO of VCCIO6 will be damaged!

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Geniatech	Geniatech Electronics Co., Ltd
Project:	RK3566_BOX_Demo1_DDR4P408DD4
File:	14.RK3566_VI Interface
Date:	Thursday, January 12, 2023
Rev:	<Revision>
Designed by:	<designer>
Reviewed by:	<Checker>
Sheet:	15 of 30

RK3566_K(VCCIO4 Domain)

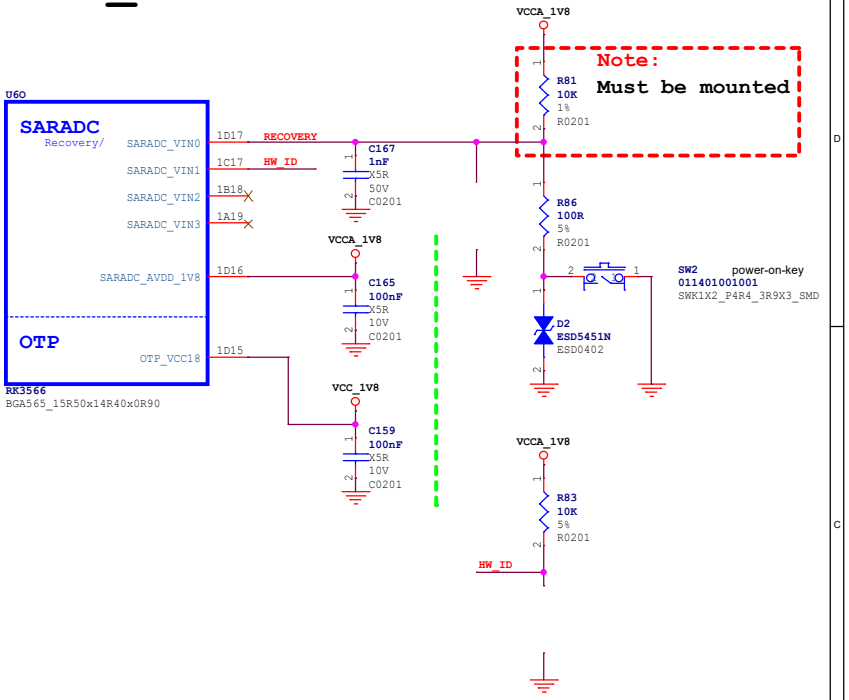


If a board needs to be compatible with two voltage choices, recommended to enable HW_ID

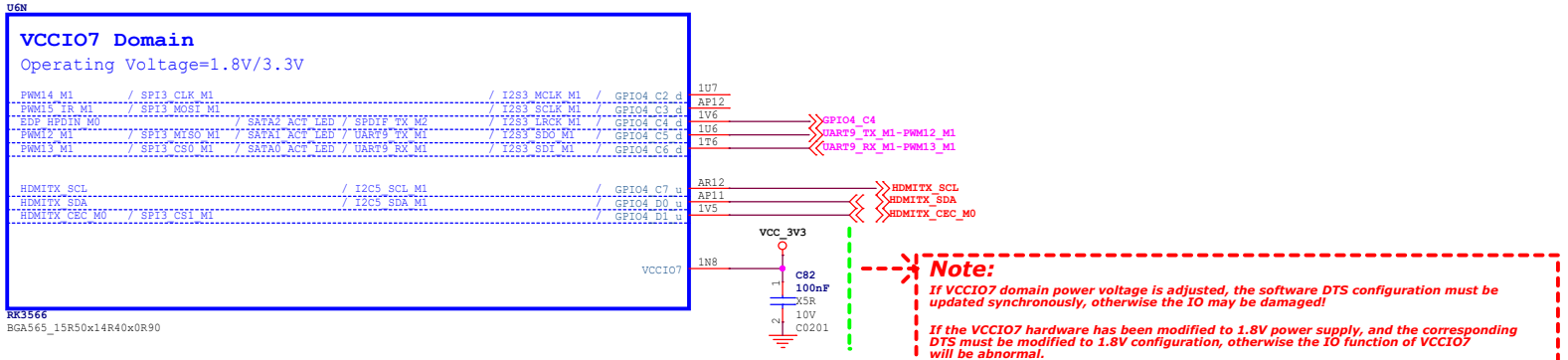
Note:

If VCCIO4 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!
If the VCCIO4 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO4 will be abnormal.
The VCCIO4 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, otherwise the IO of VCCIO4 will be damaged!

RK3566_O(SARADC/OTP)



RK3566_N(VCCIO7 Domain)



Note:

If VCCIO7 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO7 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO7 will be abnormal.

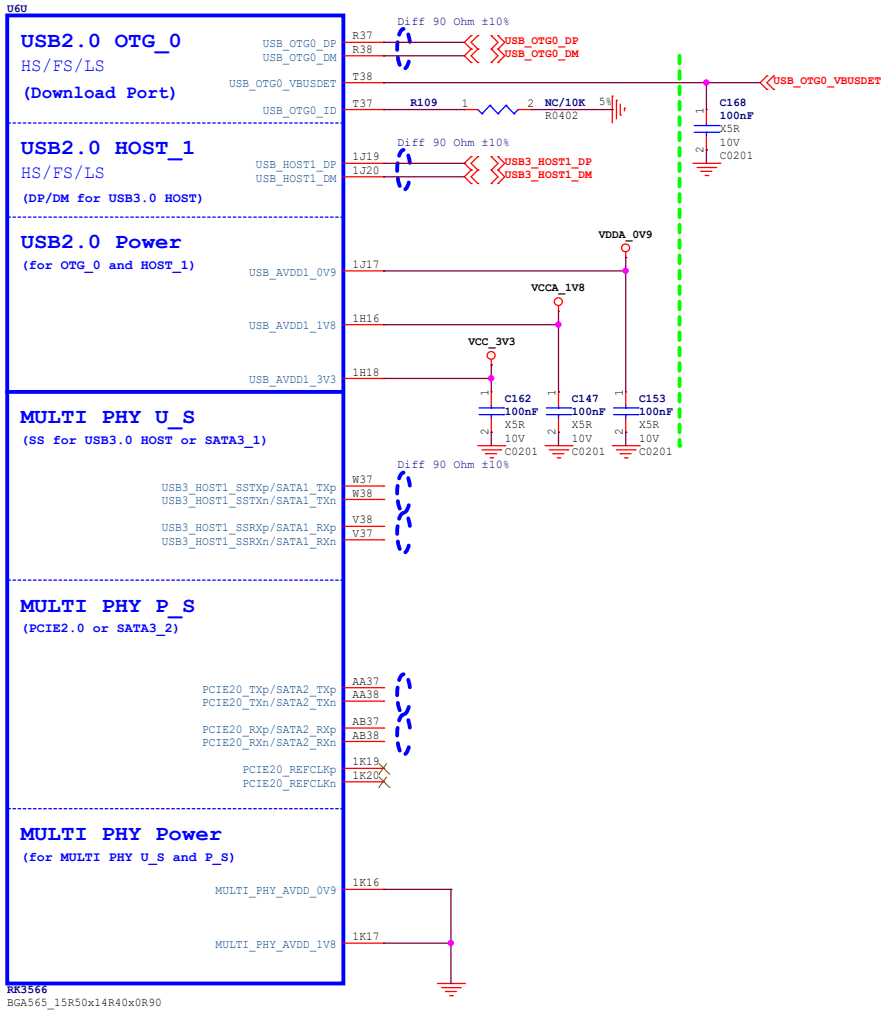
The VCCIO7 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, otherwise the IO of VCCIO7 will be damaged!

Note:

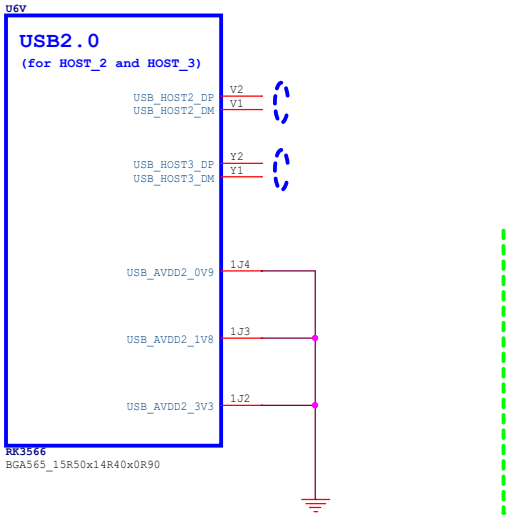
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	13.RK3566_SARADC/GPIO				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	14 of 30

RK3566_U(USB3.0/PCIe2.0 x1)



RK3566_V(USB2.0 HOST)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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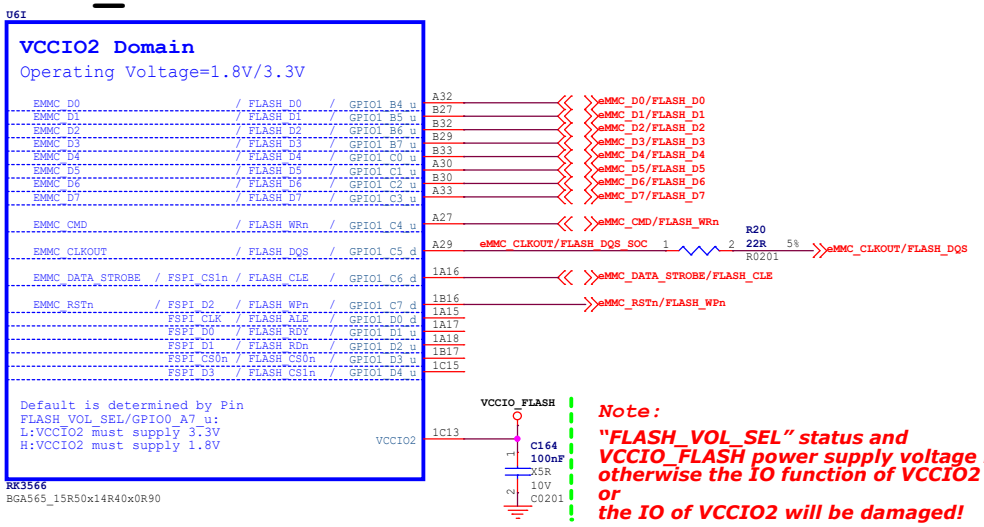
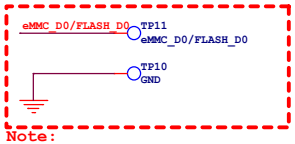
Geniatech Geniatech Electronics Co., Ltd					
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	12.RK3566_USB/PCIe PHY				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	13 of 30

RK3566_I(VCCIO2 Domain)

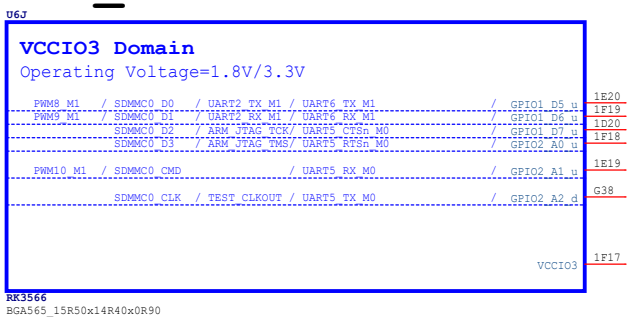




Note:
Reserve TestPoint for put the system into Maskrom mode to update the firmware

Note:
"FLASH_VOL_SEL" status and
VCCIO_FLASH power supply voltage must match
otherwise the IO function of VCCIO2 will be abnormal.
or
the IO of VCCIO2 will be damaged!

RK3566_J(VCCIO3 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

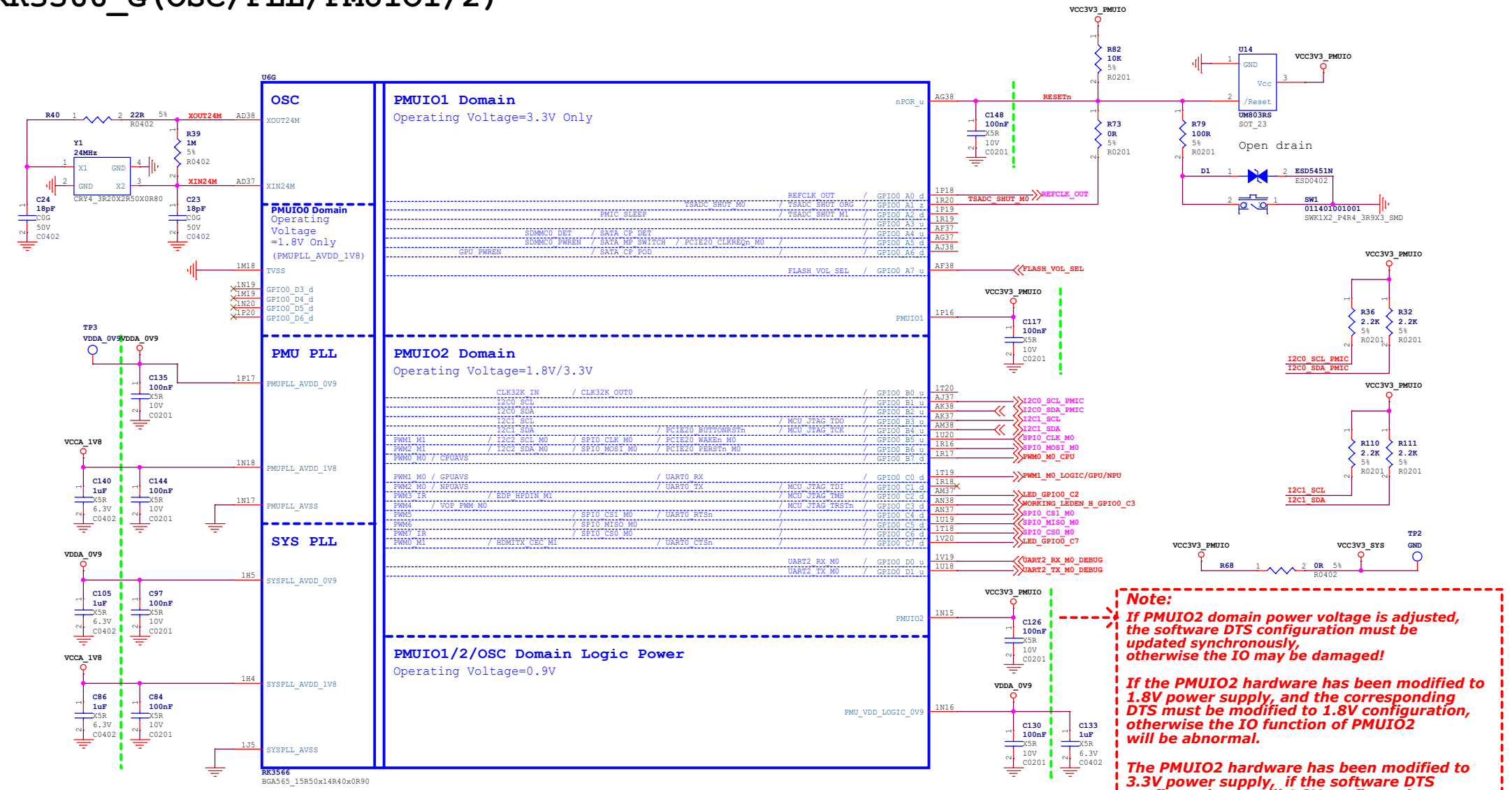
Note:
If VCCIO3 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO3 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO3 will be abnormal.

The VCCIO3 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, otherwise the IO of VCCIO3 will be damaged!

Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	11.RK3566_Flash/SD Controller				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	12 of 30

RK3566_G(OSC/PLL/PMUIO1/2)



Note:

If PMUIO2 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the PMUIO2 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of PMUIO2 will be abnormal.

The PMUIO2 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, otherwise the IO of PMUIO2 will be damaged!

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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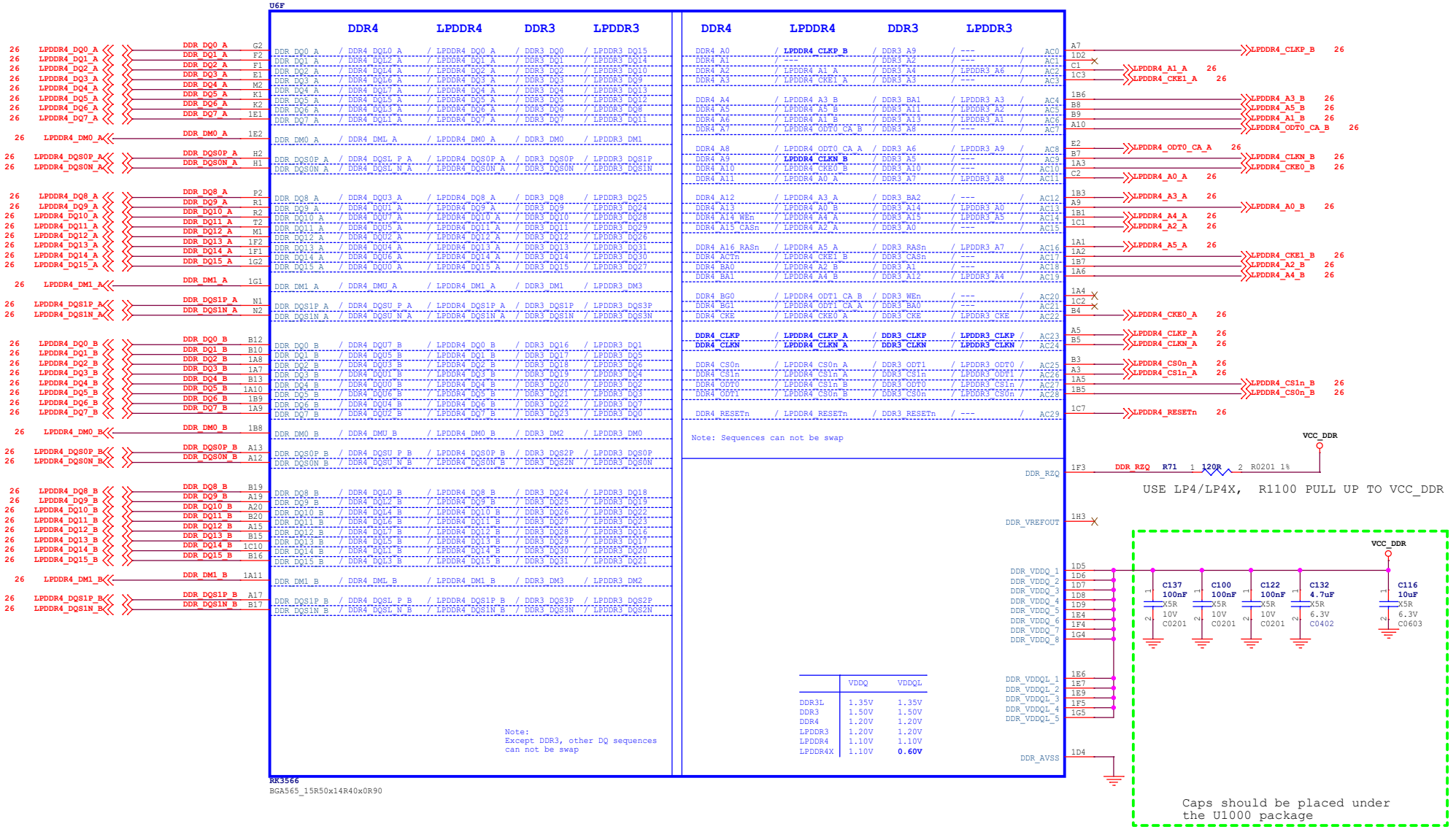
Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	10.RK3566_OSC/PLL/PMUIO				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	11 of 30

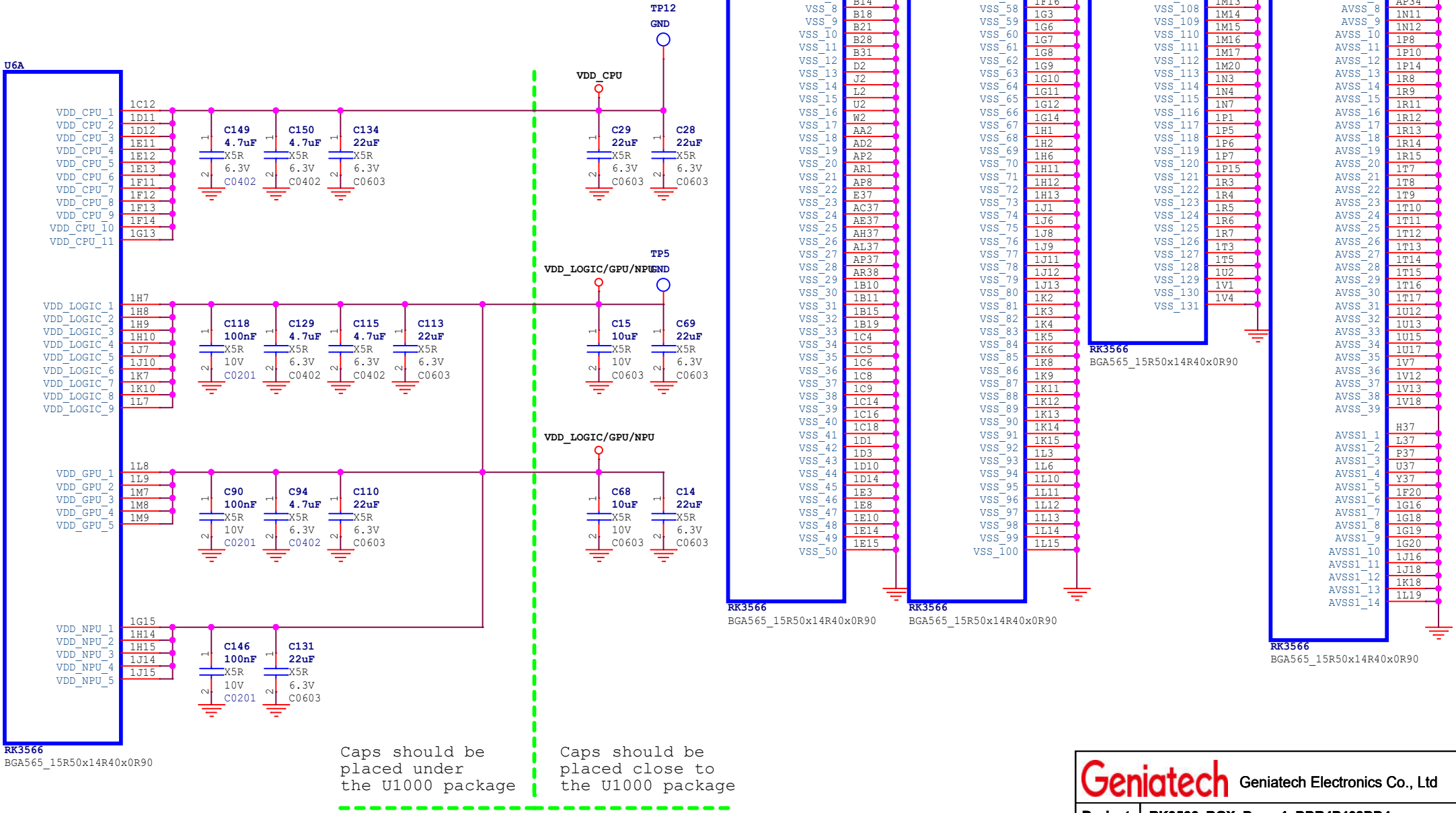
RK3566_F(DDR PHY)



Geniatech	Geniatech Electronics Co., Ltd		
Project:	RK3566_BOX_Demo1_DDR4P408DD4		
File:	09.RK3566_DDR PHY		
Date:	Thursday, January 12, 2023	Rev:	<Revision>
Designed by:	<designer> Reviewed by: <Checker>	Sheet:	10 of 30

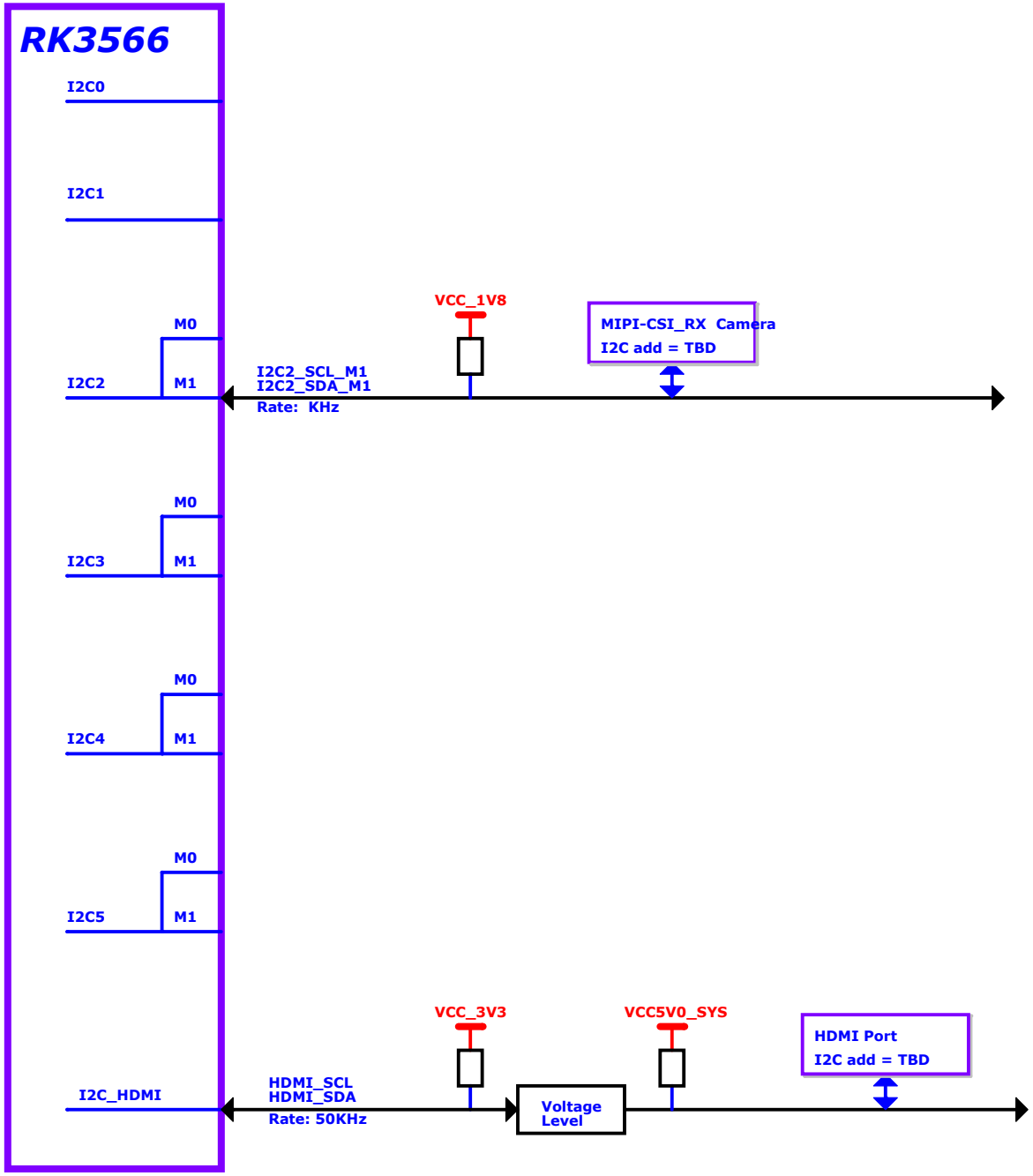
RK3566_ABCDE

(Power&GND)



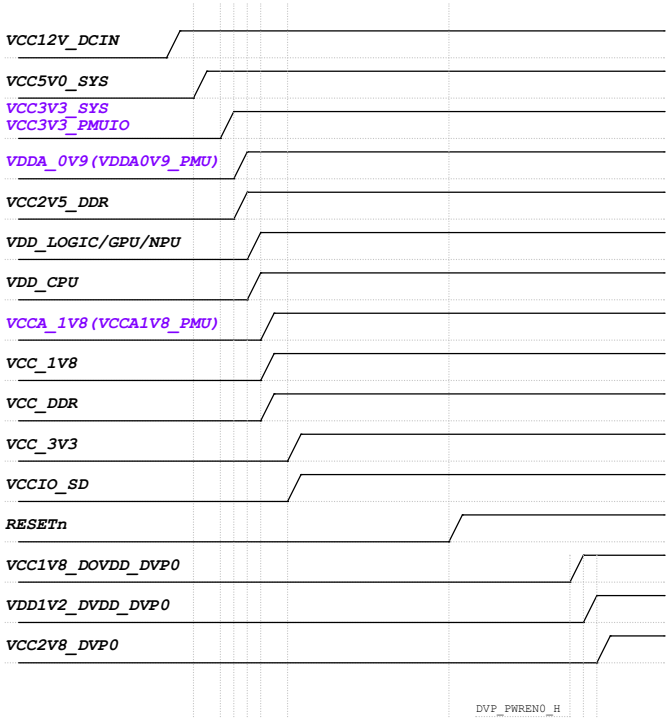
Geniatech Geniatech Electronics Co., Ltd					
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	08.RK3566_Power/GND				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	9 of 30

I2C MAP



Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	07.I2C Bus Map				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	8 of 30

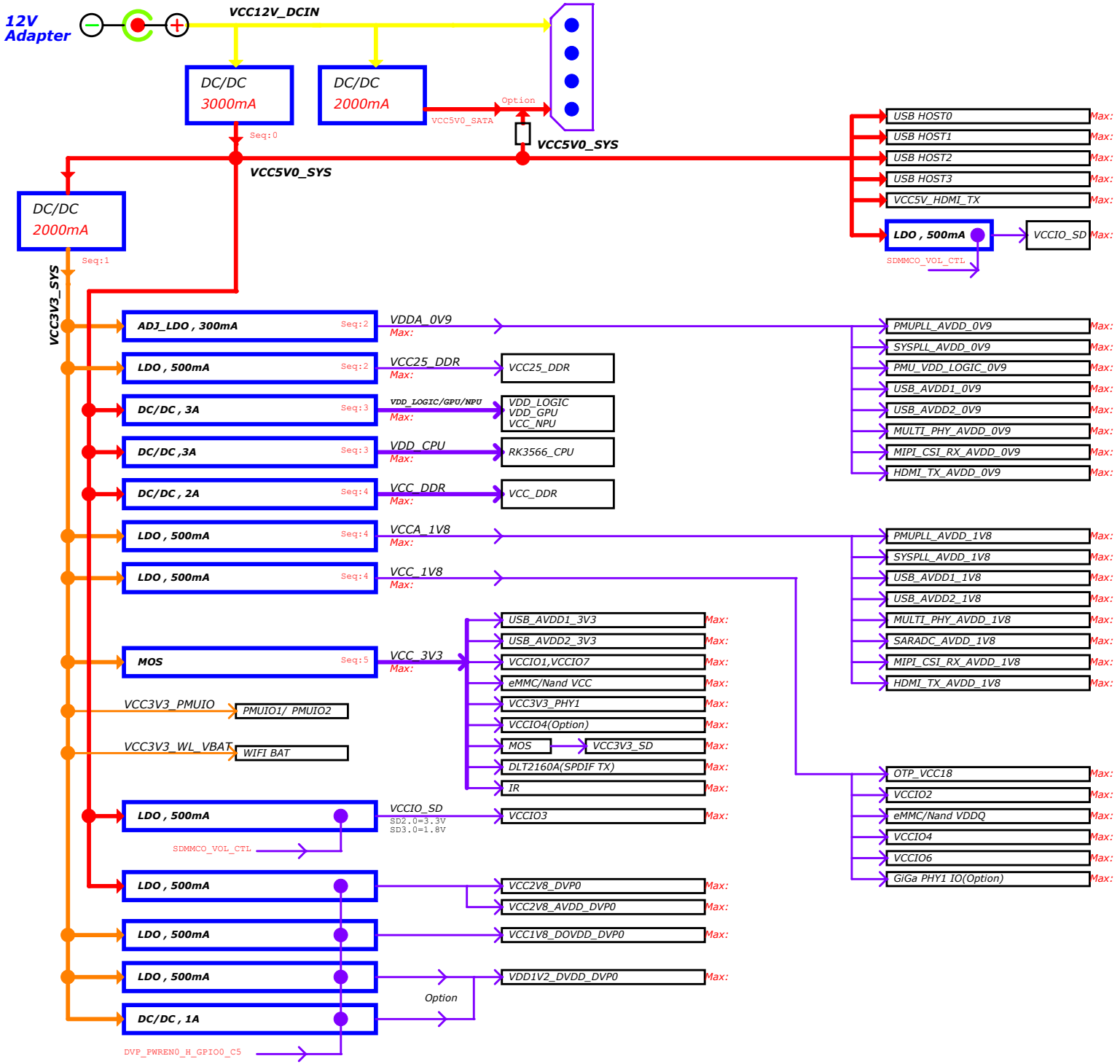
Power Sequence



Power Supply	Channel	Supply Limit	Power Name	Time Slot	Default Voltage
VCC12V_DCIN	BUCK	3.0A	VCC5V0_SYS	Slot:0	3.3V
VCC12V_DCIN	BUCK	3.0A	VCC3V3_SYS	Slot:1	5.2V
VCC3V3_SYS			VCC3V3_PMUIO	Slot:1	3.3V
VCC3V3_SYS	LDO	0.3A	VDDA_0V9	Slot:2	0.9V
VCC3V3_SYS	LDO	0.3A	VCC2V5_DDR	Slot:2	2.5V
VCC5V0_SYS	BUCK	3.0A	VDD_LOGIC/GPU/NPU	Slot:3	0.9V
VCC5V0_SYS	BUCK	5.0A	VDD_CPU	Slot:3	0.9V
VCC3V3_SYS	LDO	0.5A	VCC_1V8	Slot:4	1.8V
VCC3V3_SYS	LDO	0.5A	VCCA_1V8	Slot:4	1.8V
VCC5V0_SYS	BUCK	1.5A	VCC_DDR	Slot:4	1.2V DDR4
VCC3V3_SYS	MOS	2A	VCC_3V3	Slot:5	3.3V
VCC5V0_SYS	LDO	0.5A	VCCIO_SD	Slot:5A	3.3V
VCC3V3_PMUIO	RESETn				
VCC3V3_SYS	LDO	0.5A	VCC1V8_DOVDD_DVP0		1.8V
VCC3V3_SYS	LDO or BUCK	0.5A/1A	VDD1V2_DVDD_DVP0		1.2V
VCC5V0_SYS	LDO	0.5A	VCC2V8_DVP0		2.8V

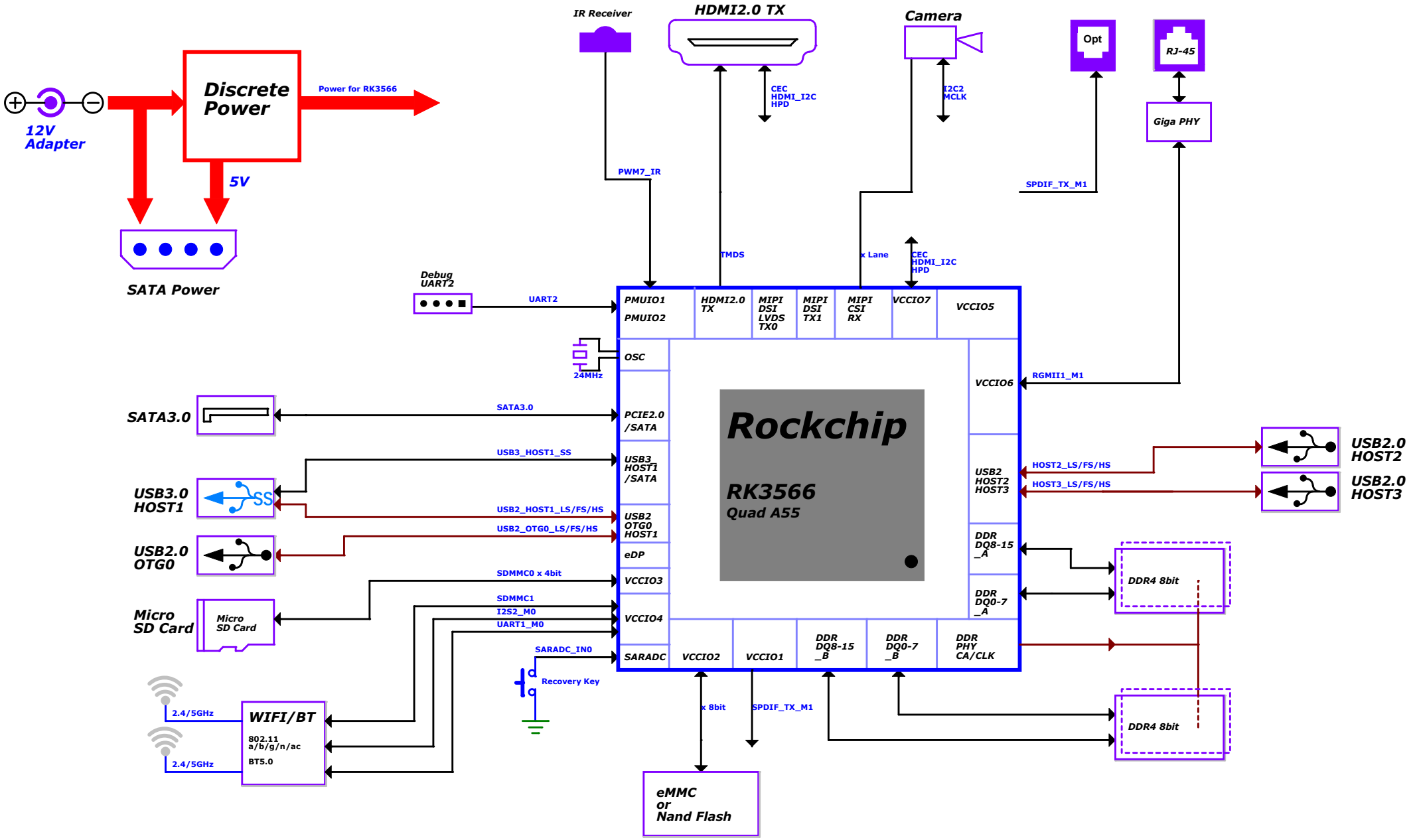
Geniatech Geniatech Electronics Co., Ltd					
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	05.Power Sequence				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	6 of 30

Power Diagram



Geniatech	Geniatech Electronics Co., Ltd
Project:	RK3566_BOX_Demo1_DDR4P408DD4
File:	04.Power Diagram
Date:	Thursday, January 12, 2023
Rev:	<Revision>
Designed by:	<designer>
Reviewed by:	<Checker>
Sheet:	5 of 30

RK3566 Ref Block Diagram



Geniatech	Geniatech Electronics Co., Ltd
Project:	RK3566_BOX_Demo1_DDR4P408DD4
File:	03.Block Diagram
Date:	Thursday, January 12, 2023
Rev:	<Revision>
Designed by:	<designer>
Reviewed by:	<Checker>
Sheet:	4 of 30

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-01-05	Zhangdz	1:Revision preliminary version	
V1.1	2021-01-27	Zhangdz	1:Add DDR4 8bit supports CS1/ODT1 2:Change IR to PWM3_IR	
V1.2	2021-06-07	Zhangdz	1:Add IO domain description 2:Update DDR4 PCB package library, compatible with large capacity DDR4	

Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	01.Index and Notes				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	2 of 30

Schematics For RK3566 BOX

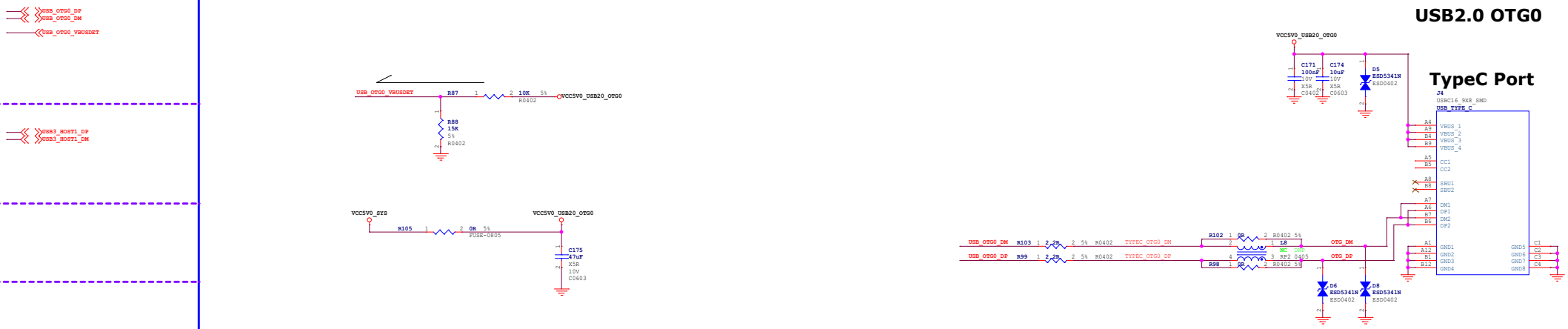
RK3566_BOX_Demo1_DDR4P408DD4_V12

Main Functions Introduction

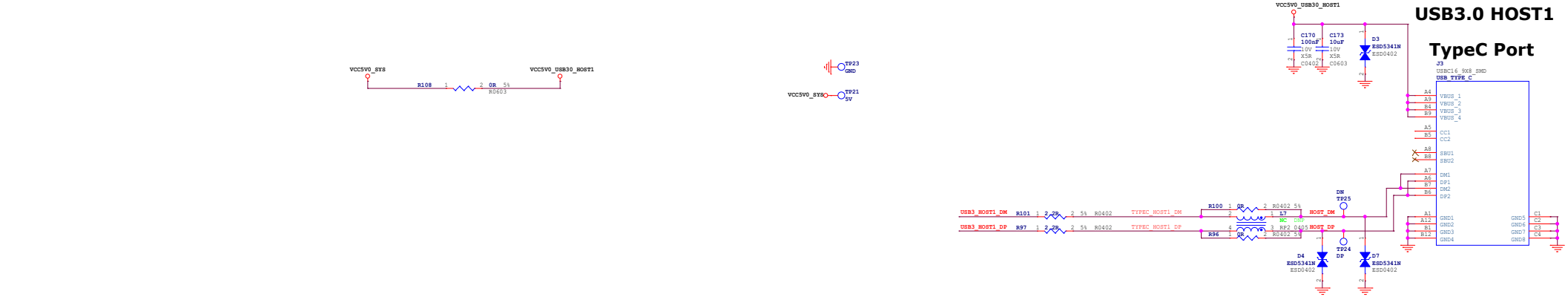
1) PMIC: DiscretePower(DCIN 12V)
2) RAM: DDR4 4x8Bit
3) ROM: eMMC,Nand Flash(Option)
4) Support: 1 x Micro SD Card3.0
5) Support: 1 x SATA3.0 Connector (7pin)
6) Support: 1 x USB2.0 OTG + 1 x USB3.0 HOST + 2 x USB2.0 HOST
7) Support: 1 x HDMI2.0 TX
8) Support: 1 x Optical S/PDIF TX
9) Support: 1 x 4Lane MIPI CSI RX
10) Support: 1 x 10/100/1000 Ethernet(RGMII)
11) Support: 1 x a/b/g/n/ac Wi-Fi + BT 5.0(2T2R)
12) Support: 1 x IR Receiver
13) Support: 1 x Recovery Key
14) Support: 1 x Power LED,1 x Working LED,1 x IR LED,1 x SATA ACT LED
15) Support: Debug UART

Geniatech Geniatech Electronics Co., Ltd					
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	00.Cover Page				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	1 of 30

USB2.0 OTG0



USB3.0 HOST1



USB2.0 HOST2

USB2.0 HOST3

Geniatech Geniatech Electronics Co., Ltd			
Project:	RK3566_BOX_Demo1_DDR4P408DD4		
File:	21.USB2/USB3 Port		
Date:	Thursday, January 12, 2023	Rev:	<Revision>
Designed by: <designer>	Reviewed by: <Checker>	Sheet:	22 of 30

IO Power Domain Map

If IO domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

IO Domain	Pin Num	Support IO Voltage		Notes	Default IO Domain Voltage		
		3.3V	1.8V		Supply Power Net Name	Power Source	Voltage
PMUIO0 (PMUPLL_AVDD_1V8)	Pin 1N18	✗	✓	PMUIO0 are fixed 1.8V level mode, which cannot be configured.	VCCA_1V8	VCCA_1V8	1.8V
PMUIO1	Pin 1P16	✓	✗	PMUIO1 are fixed 3.3V level mode, which cannot be configured.	VCC3V3_PMUIO	VCC3V3_SYS	3.3V
PMUIO2	Pin 1N15	✓	✓	PMUIO2 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC3V3_PMUIO	VCC3V3_SYS	3.3V
VCCIO1	Pin 1D13	✓	✓	VCCIO1 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC_3V3	VCC_3V3	3.3V
VCCIO2	Pin 1C13	✓	✓	VCCIO2 supports 1.8V or 3.3V level mode Default is configured by hardware,namely PIN "FLASH_VOL_SEL" state determines which mode to work in.[1][2]	VCCIO_FLASH	VCC_1V8	1.8V
VCCIO3	Pin 1F17	✓	✓	VCCIO3 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2][3]	VCCIO_SD	VCCIO_SD	3.3V
VCCIO4	Pin 1E16	✓	✓	VCCIO4 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO_WL	VCC_1V8	1.8V
VCCIO5	Pin 1N5 Pin 1N6	✓	✓	VCCIO5 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	NC		
VCCIO6	Pin 1L4 Pin 1L5	✓	✓	VCCIO6 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC_1V8	VCC_1V8	1.8V
VCCIO7	Pin 1N8	✓	✓	VCCIO7 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC_3V3	VCC_3V3	3.3V

For example, the VCCIO4 hardware has been modified to 3.3V power supply, and the corresponding DTS must be modified to 3.3V configuration, otherwise the IO of VCCIO4 will be damaged.

If a board needs to be compatible with two voltage choices, recommended to enable HW_ID

Notes

[1]:When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship, its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

[2]:When the IO domain power supply voltage is 1.8V, the IO domain voltage configuration in DTS must be set to 1.8V mode.
If it is misconfigured to 3.3V mode, the IO function of this power domain will be abnormally;
When the IO domain power supply voltage is 3.3V, the IO domain voltage configuration in DTS must be set to 3.3V mode.
If it is misconfigured to 1.8V mode, the IO in this power domain will be in overvoltage state, and the IO will be damaged after long-term operation.

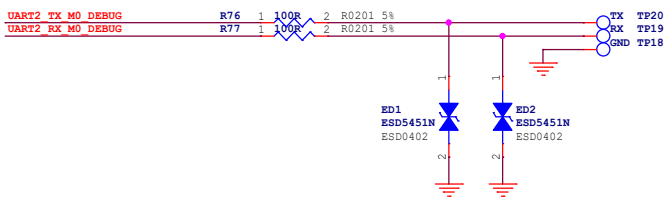
[3]:When VCCIO3 IO domain is assigned as SD card function,:
If SD3.0 mode is to be supported, VCCIO3 power supply voltage must be support configurable, 3.3V in SD2.0 mode and 1.8V in SD3.0 mode.
If only SD2.0 mode is supported (SD3.0 card only works in SD2.0 mode), VCCIO3 only needs fixed power supply of 3.3V.
When VCCIO3 IO domain is assigned as other function,:
Such as uart5 and uart6, then note [2] should be followed

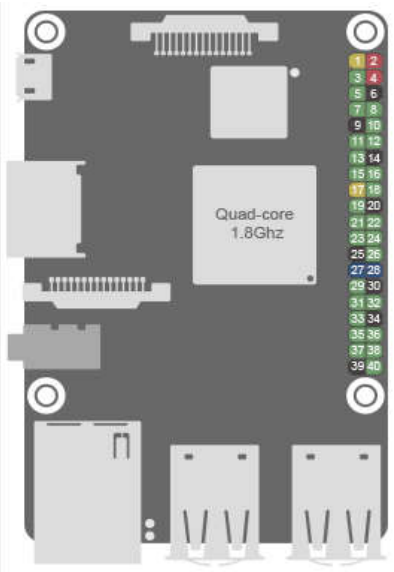
UART2_RX_M0_DEBUG

UART2_TX_M0_DEBUG

Debug UART2

default 3.3V





1	VCC3.3V_IO	2	VCC5V_SYS
3	GP8A4_I2C1_SDA	4	VCC5V_SYS
5	GP8A5_I2C1_SCL	6	GND
7	GP0C1_CLKOUT	8	GP5B1_UART1TX
9	GND	10	GP5B0_UART1RX
11	GP5B4_SPI0CLK_UART4CTSN	12	GP6A0_PCM/I2S_CLK
13	GP5B6_SPI0_TXD_UART4TX	14	GND
15	GP5B7_SPI0_RXD_UART4RX	16	GP5B2_UART1CTSN
17	VCC33_IO	18	GP5B3_UART1RTSN
19	GP8B1_SPI2TXD	20	GND
21	GP8B0_SPI2RXD	22	GP5C3
23	GP8A6_SPI2CLK	24	GP8A7_SPI2CSN0
25	GND	26	GP8A3_SPI2CSN1
27	GP7C1_I2C4_SDA	28	GP7C2_I2C4_SCL
29	GP5B5_SPI0CSN0_UART4RTSN	30	GND
31	GP5C0_SPI0CSN1	32	GP7C7_UART2TX_PWM3
33	GP7C6_UART2RX_PWM2	34	GND
35	GP6A1_PCM/I2S_FS	36	GP7A7_UART3RX
37	GP7B0_UART3TX	38	GP6A3_PCM/I2S_SDI
39	GND	40	GP6A4_PCM/I2S_SDO

REFCLK_OUT

I2C1_SCL

I2C1_SDA

I2C3_SCL_M0

I2C3_SDA_M0

I2S2 Change To I2S1

I2S1_SCLK_TX_M1

I2S1_LRCK_TX_M1

I2S1_SDO0_M1

I2S1_SDI0_M1

UART1_RX_M1

UART1_TX_M1

UART1_RTSn_M1

UART1_CTSn_M1

UART4_RX_M0

UART4_TX_M0

UART4_CTSn_M0

UART4_RTSn_M0

UART7_TX_M2

UART7_RX_M2

UART9_TX_M1-PWM12_M1

UART9_RX_M1-PWM13_M1

GPIO4_C4

SPI0_CS0_M0

SPI0_CS1_M0

SPI0_CLK_M0

SPI0_MOSI_M0

SPI0_MISO_M0

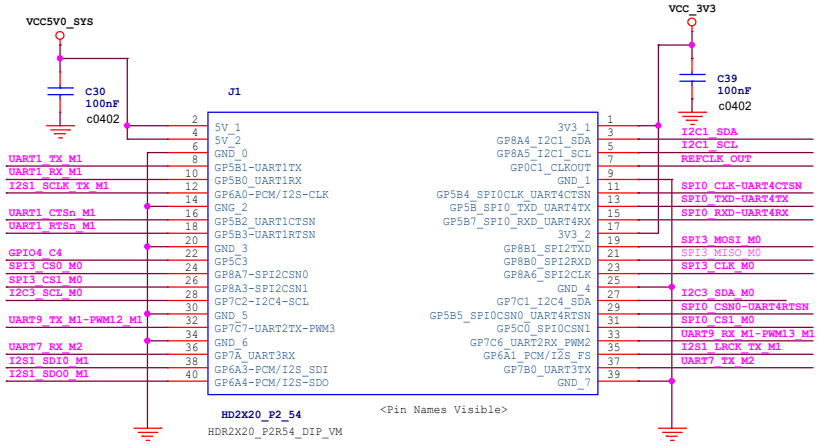
SPI3_CS1_M0

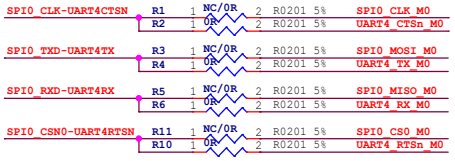
SPI3_CS0_M0

SPI3_MOSI_M0

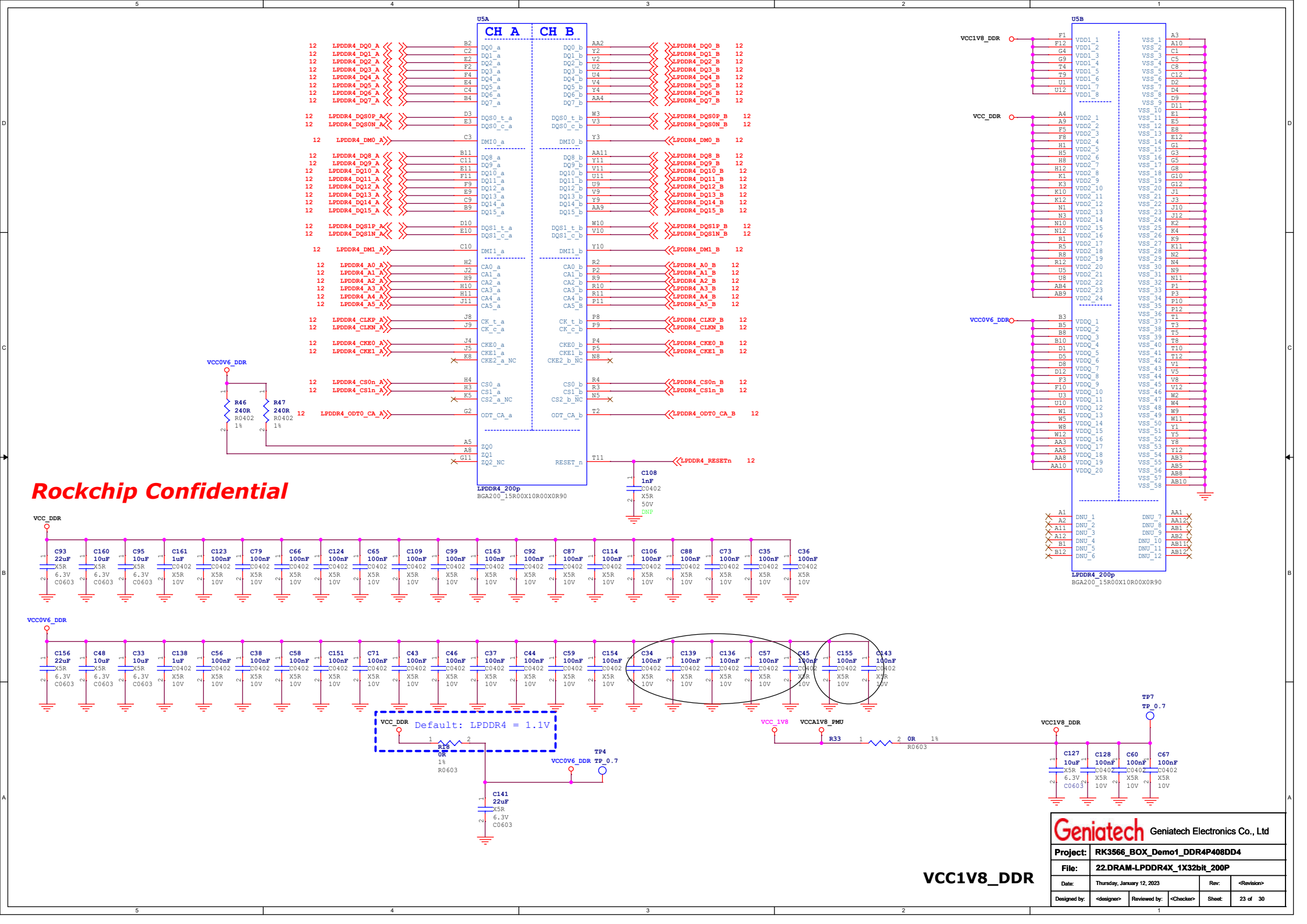
SPI3_MISO_M0

SPI3_CLK_M0





Geniatech	Geniatech Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	27.40pin-Header & UART				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	28 of 30



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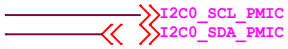
Geniatech	Geniatech Electronics Co., Ltd
Project:	RK3566_BOX_Demo1_DDR4P408DD4
File:	22.DRAM-LPDDR4X_1X32bit_200P
Date:	Thursday, January 12, 2023
Rev:	<Revision>
Designed by:	<designer>
Reviewed by:	<Checker>
Sheet:	23 of 30

VCC1V8_DDR

EEPROM



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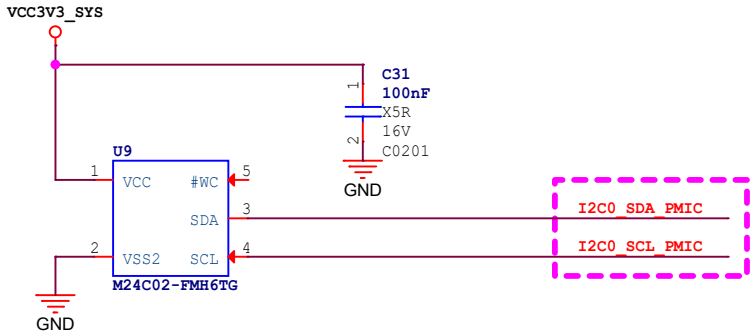

Encryption IC

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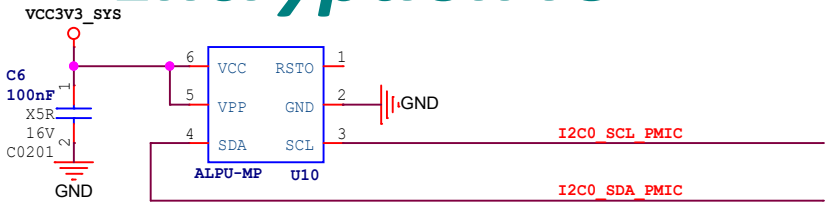

Geniatech Geniatech Electronics Co., Ltd					
Project:	**RK3566_BOX_Demo1_DDR4P408DD4**				
File:	**28.EEPROM&Encryption IC**				
Date:	Thursday, January 12, 2023			Rev:	<Revision>
Designed by:	<designer>	Reviewed by:	<Checker>	Sheet:	29 of 30